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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,439	12/28/2001	Alankar Saxena	42390.P12921	9304

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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,439	SAXENA ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sita, et al, U.S. Patent 6,301,299 and Howe, U.S. Patent 5,900,865.

5. Regarding claim 1, representative of claims 26-30 and 33, Sita discloses a method for storing a block of data on first and second memory channels in an interleaved pattern (Column 6, lines 19-38; Column 22, lines 6-8; Column 5, line 52; Column 2, line 65; Column 20, line 2) comprising: receiving a set of parameters that describe the block of data from a source (Column 7, lines 1-29; Column 23, lines 50-58); determining a request address based on the parameters (Column 15, lines 62-65); translating the request address to corresponding first and second address channels based upon the parameters, further comprising: determining, based upon selected address bits (), a corresponding address for the first channel; adding an offset to the first address channel to produce a address for the second channel (Column 23, lines 10-17; Column 24, lines 25-65; Table 8*(see Claim 6)*); and storing portions of the block of data in accordance with the first and second addresses such that selected portions of the block of data are accessible at the same time (Column 16, line 10) via first and second memory channels;

[further claim 30] a block of image data (*macroblocks,* Figure 2A; Column 5, lines 19-32) in an interleaved pattern among a first and second channel (see above), comprising: a processor (Column 5, line 22); a memory operably coupled to the processor (Column 5, lines 19-22), wherein the memory stores a mapping algorithm (Figure 1E, Column 2, lines 58-61) and a block of data (Column 1, lines 33-40), wherein when executed by the processor the mapping algorithm causes the processor to perform the function of (see above).

[further claim 28] MPEG decoder, MPEG video data (Column 2, lines 58-61).

[further claim 29] memory controller (Column 1, lines 13-15).

Sita does not disclose further comprising: determining, based upon selected address bits, a corresponding address for the first channel; an apparatus for tiling a block of image data; tiled;

tiled address channels; tiled address bits. Howe teaches further comprising: determining, based upon selected address bits, a corresponding address for the first channel; an apparatus for tiling a block of image data; tiled; tiled address channels; tiled address bits (Column 11, lines 56-67; Column 12, lines 1-36; Column 14, lines 25-28; Column 16, lines 3-26). The motivation for combining interleaved memory storage using multiple channels with tiles and tiled address bits is for faster access time resulting from efficient retrieval of pixels by macroblocks without crossing a DRAM page boundary (Column 11, lines 4-5, 20-24). Howe is evidence that at the time of the invention, it would have been obvious to one skilled in the art or MPEG video processing to combine the benefits of interleaved memory storage using multiple channels, as Sita discloses, with tiling and bit addressing, as Howe teaches, for faster processing speeds and efficient memory utilization.

6. Regarding claim 2, representative of claims 6, 10, 14, 18, 22, 31, 32, 34 and 35, Sita discloses the method of claim 1, wherein the request address is directed to a X/Y-major format tile and X/Y-walk data request (Figures 20-21; *horizontal and vertical motion vectors,* Column 25, lines 35-50).

Sita does not disclose an apparatus for tiling a block of image data; tiled; tiled address channels; tiled address bits. Howe teaches an apparatus for tiling a block of image data; tiled; tiled address channels; tiled address bits (Column 11, lines 56-67; Column 12, lines 1-36; Column 14, lines 25-28; Column 16, lines 3-26). The motivation for combining interleaved memory storage using multiple channels with tiles and tiled address bits is for faster access time resulting from efficient retrieval of pixels by macroblocks without crossing a DRAM page

boundary (Column 11, lines 4-5, 20-24). Howe is evidence that at the time of the invention, it would have been obvious to one skilled in the art or MPEG video processing to combine the benefits of interleaved memory storage using multiple channels, as Sita discloses, with tiling and bit addressing, as Howe teaches, for faster processing speeds and efficient memory utilization.

7. Regarding claim 3, representative of claims 7, 11, 15, 19, and 23, Sita discloses the method of claim 2, wherein the block of data is comprised of an aligned Hword (hexword, 32 bytes); two adjacent Owords (octword, 8x2, 16 bytes); two Owords skipping one; aligned Oword on a scan line; two Owords; four adjacent Qwords (4x8, 32 bytes) (downsampling, decimation, Figures 3B, 4, 14-15; Column 11, lines 29-48).

8. Regarding claim 4, representative of claims 5, 8, 9, 12, 13, 16, 17, 20, 21, 24, 25, Sita discloses a method of claim 3, wherein the first address channel equals the request address and the second address channel, request address+16B/ +128B/ +256B (*64-bit words, quadwords,* Figures 10-12, 16-17; Column 20, lines 15 through Column 27, line 34).

Sita does not disclose equals the request address+16B responsive to: (Tiled Address [8]="0" AND Tiled Address [7]="0") or (Tiled Address [8]="1" AND Tiled Address [7]="1");

[claim 5] (Tiled Address [8]="0" AND Tiled Address [7]="1") or (Tiled Address [8]="1" AND Tiled Address [7]="0");

[claim 8] the first tiled address channel equals the request address and the second tiled address channel equals the request address+128 B responsive to: (Tiled Address [4]="0" AND Tiled Address [8]="0") or (Tiled Address [4]="1" AND Tiled Address [8]="1");

[claim 9] the first tiled address channel equals the request address+128K and the second tiled address channel equals the request address responsive to: (Tiled Address [4]="0" AND Tiled Address [8]="1") or (Tiled Address [4]="1" AND Tiled Address [8]="0").

[claim 12] the first tiled address channel equals the request address and the second tiled address channel equals the request address+256 B responsive to: (Tiled Address [4]="0" AND Tiled Address [7]="0") or (Tiled Address [4]="1" AND Tiled Address [7]="1").

[claim 13] the first tiled address channel equals the request address+256 K and the second tiled address channel equals the request address responsive to: (Tiled Address [4]="0" AND Tiled Address [7]="1") or (Tiled Address [4]="1" AND Tiled Address [7]="0").

[claim 16] wherein responsive to (Tiled Address [5]="0" AND Tiled Address [4]="0") or (Tiled Address [5]="1" AND Tiled Address [4]="1") Channel 0=Request Address Qword (Tiled Address [3])=Qword 0 of Source Qword (Tiled Address [3])=Not Used/Updated Channel 1=Request Address+128B Qword (Tiled Address [3])=Qword 1 of Source Qword (Tiled Address [3])=Not Used/Updated.

[claim 17] wherein responsive to (Tiled Address [5]="0" AND Tiled Address [4]="1") or (Tiled Address [5]="1" AND Tiled Address [4]="0") Channel 0=Request Address+128B Qword (Tiled Address [3])=Qword 1 of Source Qword (Tiled Address [3])=Not Used/Updated Channel 1=Request Address Qword (Tiled Address [3])=Qword 0 of Source Qword (Tiled Address [3])=Not Used/Updated.

[claim20] wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address+128 B responsive to: (Tiled Address [5]="0" AND Tiled Address [4]="0") or (Tiled Address [5]="1" AND Tiled

Address [4]="1"); [claim 21] wherein the first tiled address channel equals the request address+128 B and the second tiled address channel equals the request address responsive to: (Tiled Address [5]="0" AND Tiled Address [4]="1") or (Tiled Address [5]="1" AND Tiled Address [4]="0").

[claim 24] wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address+16B responsive to: (Tiled Address [7]="0" AND Tiled Address [5]="0") or (Tiled Address [7]="1" AND Tiled Address [5]="1"); [claim 25] wherein the first tiled address channel equals the request address+16B and the second tiled address channel equals the request address responsive to: (Tiled Address [7]="0" AND Tiled Address [5]="1") or (Tiled Address [7]="1" AND Tiled Address [5]="0").

Sita does not disclose an apparatus for tiling a block of image data; tiled; tiled address channels; tiled address bits. Howe teaches an apparatus for tiling a block of image data; tiled; tiled address channels; tiled address bits (Column 11, lines 56-67; Column 12, lines 1-36; Column 14, lines 25-28; Column 16, lines 3-26). The motivation for combining interleaved memory storage using multiple channels with tiles and tiled address bits is for faster access time resulting from efficient retrieval of pixels by macroblocks without crossing a DRAM page boundary (Column 11, lines 4-5, 20-24). Howe is evidence that at the time of the invention, it would have been obvious to one skilled in the art or MPEG video processing to combine the benefits of interleaved memory storage using multiple channels, as Sita discloses, with tiling and bit addressing, as Howe teaches, for faster processing speeds and efficient memory utilization.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

***October 30, 2003

Matthew C. Bella

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